Table 2-2. Roller Indicators

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
1	1	0–3	SCON SATR SEL	KR 051	SATR or SCON from CE 1–4.
1	1	4	TIME CLOCK STEP	KD 601	Time clock step trigger.
1	1	18–26	G REGISTER (WRITE DIRECT)	RG 001	Contents of G register.
1	1	27–35	ADDRESS TRANSLATION REGISTER	FA 091	Contents of ATR (32–29).
1	2	0–8	F REGISTER (READ DIRECT)	RF 001	Contents of F register.
1	2	9–35	D REGISTER	RD 001	Contents of D register.
1	3	0–35	S REGISTER	RS 001	Contents of S register.
1	4	0–11	READ ONLY STORAGE ADDRESS REGISTER	RX 021	Contents of ROSAR.
1	4	12–23	ROS PREVIOUS ADDRESS REGISTER A	RX 211	Contents of previous ROS address register A, (PROSARA).
1	4	24–35	ROS PREVIOUS ADDRESS REGISTER B	RX 211	Contents of previous ROS address register B, (PROSARB).
1	5	0–35	SELECT REGISTER	FS 001	Contents of select register.
1	6	0–35	L or M REGISTER	XL 031	Contents of L or M register (selected by IND RLR 1 switch).
2	1	0–35	ADDRESS TRANSLATION REGISTER 1	FA 111	Contents of ATR (0–31).
2	2	0	E REG PTY	RE 181	Parity error in E (0–15).
2	2	1–9	PADD FULL SUM	AP 075	Full-sum parity error.
2	2	18	MLPR DECODE PTY	DP 091	Parity error in multiplier (S register).
2	2	19–26	PADD HALF-SUM	AP 791	Half-sum parity error.
2	2	27	ERROR TGR	AP 801	Half-sum error.
2	2	31–33	ROS PTY	DS 431	ROS parity error.
2	2	34,35	SADD	AS 095	Half-sum or full-sum error in serial adder.
2	3	0–35	T REGISTER	RT 321	T register contents.
2	4	2–5	FAA CONTROLS	RY 015	Miscellaneous control lines.
2	4	6–9	AB, IC INGATES	RY 021	Ingating to A,B,IC.
2	4	10,11	LS-T, LS-S	RY 031	Gate local store to S, T.
2	4	12–16	ST, D, Q, G, PSW INGATES	RY 041	Ingating to D,K,Q,S,T,PSW,N,G.
2	4	17–20	INGT AND EOP	RY 071	End ops and gate serial adder to F.
2	4	21–24	EMIT, E, R INGATES	RY 061	Emit and ingating to E,R.
2	4	25–30	MISC CONTROL PART 2	RY 101	Miscellaneous control lines.
2	4	31–35	MISC CONTROL PART 1	RY 081	Set IC and miscellaneous control lines.
2	5	0–35	X REGISTER	XX 031	Contents of X register.
2	6	0–35	K REGISTER	RK 001	Contents of K register.
3	1	0–5	STORAGE REQUEST	MC 061	Source of storage request.
3	1	6	PAGE 1 LTH	MC 991	Forced storage cycle for address of new page.
3	1	9	RPT INSN ADJ	KW 051	Repeat INSN switch in SINGLE or MPLE with CE in stopped status.
3	1	10	RPT INSN INIT	KW 051	CE executing instructions with REPEAT INSN switch in SINGLE or MPLE.
3	1	11	PULSE MODE ADJ	KW 061	PULSE MODE switch in TIME or COUNT.
3	1	12	PULSE MODE INIT	KW 061	CE executing instructions with PULSE MODE switch in TIME or COUNT.
3	1	13	STOP	KW 031	CE is operating in the stop loop.
3	1	14	BLOCK	KW 041	'Block' trigger is set, which allows one clock cycle to be gated to CE logic each time START is depressed when in single-cycle mode (RATE switch in SINGLE CYCLE or SINGLE CYCLE STORAGE INHIBIT).

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
3	1	15	PASS PULSE	KW 041	'Pass pulse' trigger is set, which gates clock cycles to CE logic in single-cycle mode (RATE switch in SINGLE CYCLE or SINGLE CYCLE STORAGE INHIBIT).
3	1	16	BLOCK IRPT	KW 021	Block interrupts during 'reset stop triggers' cycle or during 'ROS decode I-fetch reset' cycle.
3	1	17	FORCE ADR	KC 031	'Force address' trigger set by 'pulse mode singleshot', 'load' or 'reset' and used to set ROSAR (11).
3	1	18	INSN STEP	KW 021	RATE switch in INSN STEP and CE in manual state.
3	1	19	SINGLE CYCLE	KW 021	RATE switch in SINGLE CYCLE or SINGLE CYCLE STORAGE INHIBIT and CE in manual state.
3	1	20	CHK SUMM	KW 081	Any error latch set.
3	1	21	INHIB CLOCK	KC 011	Inhibit clock from BCU or FLT controls.
3	1	22	REPEAT TEST	KU 311	TEST MODE REPEAT switch in REPEAT causes CE to repeat ROS test or FLT in main storage.
3	1	23	FLT TEST	KU 291	TEST MODE switch in FLT.
3	1	24	ROS TEST	KU 331	TEST MODE switch in ROS.
3	1	25	SCC	KU 331	'Scan counter control' trigger set.
3	1	26	SYNC	KU 371	FLT sync trigger set.
3	1	27	NO REV	KU 031	'Disable interleaving' latch set by diagnose instruction bit 8 (I-field).
3	1	28	REV	KU 031	'Disable interleaving and reverse storage address' latch set by diagnose instruction bit 9 (I2 field).
3	1	29	RESTART	KU 311	'Restart I/O' latch set by RESTART FLT I/O pushbutton.
3	1	30	CNSL LOG	KU 311	'Console logout' latch set by LOG OUT pushbutton.
3	1	31	SOROS	KU 351	Scan out ROS (hardware controlled) portion of logout operation is in progress or cycle counter is reduced to zero during FLT operation.
3	1	32	DIAG	KU 331	Diagnose instruction is being executed.
3	1	33	DIAG LOAD	KU 371	TEST MODE switch in ROS or FLT and CE is executing initial program load.
3	1	34	TIC	KU 291	'TIC latch' set by signal received from IOCE when IOCE decodes a CCW specifying transfer in channel.
3	1	35	GAP	KU 291	'GAP latch' set by signal received from IOCE when IOCE detects an inner record gap on tape.
3	2	0–35	Q REGISTER	RQ 001	Contents of Q register.
3	3	0–35	A REGISTER	RA 001	Contents of A register.
3	4	0–6	EXTD and LS LAR CONTROL	RY 131	Local storage and special register controls.
3	4	7–10	STOR REQ SET MARK	DR 191	Memory request and mark setting.
3	4	11–20	NEXT ROS BASE ADDRESS	DS 401	ROSAR (0–9) for next ROS address.
3	4	21–25	Y BRANCH	DS 411	Conditional branch (ROSAR bit 10 for next ROS address).
3	4	26–32	X or Z BRANCH	DS 421	Conditional and functional branches (ROS bit 11 for next ROS address).
3	4	34	PREV ADR A	RX 201	Contents of PROSARA addresses previous ROS word.
3	4	35	FLT MODE	KU 471	Scan mode trigger.
3	5	0–2	I/O	KM 321	IOCE interrupt being processed.
3	5	3–5	MACH CHK	KM 331	IOCE machine check interrupt request.
3	5	6–8	SEL IOCE	KX 111	IOCE-CE operations in progress.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
3	5	9	IOCE INTRPT REQ	KM 321	IOCE interrupt request.
2	5	10	IOCE MC REQ	KM 331	IOCE machine check interrupt being processed.
3	5	11	INTRPT GATE TGR	KX 181	Allow interrupt (ROS).
3	5	18–35	N REGISTER	XN 091	Contents of N register.
3	6	0–35	Y REGISTER	XX 351	Contents of Y register.
4	1	0–8	SYSTEM MASK CHANNEL	RW 011	I/O and external interrupts permitted.
4	1	9–13	PROTECTION KEY	RW 081	PSW storage protect key.
4	1	14	ASCII	RW 121	"USA Standard Code for Information Interchanges" mode of operation.
4	1	15	MACH CHK	RW 121	Machine check interrupts permitted.
4	1	16	WAIT	RW 121	Wait mode of operation.
4	1	17	PROB	RW 151	Problem mode of operation.
4	1	18	NO RETRY	KS 321	Instruction retry not advisable (programmer flag).
4	1	19	IC IN LSWR	KS 321	Contents of IC have been stored in LSWR.
4	1	20,21	COND CODE	RW 351	Current PSW condition code.
4	1	22–25	PSW PROGRAM MASK	RW 361	Current PSW program mask.
4	1	26	MACH CHK INTRPT	KM 121	Machine check interrupt is pending or being processed.
4	1	27	SUPV CALL INTRPT	KM 121	Supervisor call interrupt is pending (result of execution of "supervisor call" instruction).
4	1	30–33	PROGRAM INTRPT	KM 141	Program old PSW interrupt code, bits 28–31.
4	1	34,35	INTRPT PRI	KN 121	Priority assignments of current interrupt.
4	2	0–35	Q REGISTER	RQ 321	Contents of Q register.
4	3	0–35	B REGISTER	RB 321	Contents of B register.
4	4	0–4	A SIDE CTL SERIAL ADDER	AR 301	Ingating to serial adder, A side.
4	4	5–8	B SIDE CTL SERIAL ADDER	AR 801	Ingating to serial adder, B side.
4	4	9–11	PADDL CONTROL	AP 821	Ingating to parallel adder latches.
4	4	12	EW EXTD	AP 743	Block gating ST to serial adder B side.
4	4	13–15	GATE ONES PA	AP 811	Emit control for serial adder A side.
4	4	16	P 43–68	DS 411	Parity for ROS bits 43–68.
4	4	17	AB → F	AP 901	Gate contents of F to serial adder A side.
4	4	18–21	AB, IC, F → PB	RB 816	Ingating to parallel adder B side from A,B, and IC.
4	4	22	P 69–99	AP 901	Parity for ROS bits 69–99.
4	4	23–26	ST, DA → PA	RT 822	Ingating to parallel adder A side.
4	4	28–30	E, Q → PB	RQ 822	Ingating to parallel adder B side from E and Q.
4	4	32	RT DIG	KZ 321	Right digit trigger set (edit control).
4	4	33	S	KZ 321	Significant digit trigger set (edit control).
4	4	34	LEAVE	KZ 201	Character in edit control mask.
4	4	35	STEP ABC	KZ 501	Step ABC (edit control).
4	5	0–7	STATUS TRIGGERS	KS 021	Microprogram control triggers.
4	5	8	BLOCK	KD 501	Block I-fetch.
4	5	9–11	1 2 3	KD 111	I-fetch control triggers.
4	5	12	EXEC	KD 601	Execute instruction being performed.
4	5	14	PS CMPR	KD 501	Program store compare.
4	5	15	IN STOR FETCH	KD 701	I-fetch required.
4	5	16	BR INVLD ADDR	KD 701	Branch instruction execution developed invalid instruction address.
4	5	17	INVLD ADDR	KD 711	I-fetch invalid address.
4	5	18	IL NOT AVAIL	KM 851	Instruction length not available because of I-fetch storage protection check.
4	5	19–22	CE 1, CE 2	JA 211	Write direct (WD) and read direct (RD) external interrupt signals from CEs 1 and 2.
4	5	23	TC AT LIMIT	JA 201	External interrupt signal resulting from the contents of the internal timer (time clock) being reduced to zero.
4	5	24	CONS PB	JA 201	External interrupt signal resulting from the depression of INTERRUPT pushbutton.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
4	5	25–28	CE 3, CE 4	JA 211	Write direct (WD) and read direct (RD) external interrupt signals from CEs 3 and 4.
4	5	29	PIR	JA 251	Interrupt request from an IOCE.
4	5	30	DAR	JA 251	External interrupt resulting from an ELC.
4	5	31–33	PIR	KM 381	Interrupt request from an IOCE.
4	5	35	TIME GATE TGR	KX 311	Timing gate trigger for external interrupt timing.
4	6	0–35	EXTERNAL REGISTER	FE 001	Contents of external register.
5	1	0–4	PHYSICAL PSBAR	MP 111	Contents of Physical PSBAR.
5	1	5–9	PSBAR COUNTER	MP 301	Contents of PSBAR Counter.
5	1	10–22	LOGICAL PSBAR	MP 201	Contents of Logical PSBAR.
5	1	23	ALT PSBA	MP 501	PSBAR has been stepped to alternate.
5	1	28–31	SYSTEM MASK	RW 161	System mask for channels 7-A (allow I/O interrupt).
5	1	32	SE STOP	KM 158	Storage request to an SE or a DE that is stopped.
5	1	33–35	PSA LOCKOUT	KM 158	PSA lockout signal from IOCE 1–3.
5	2	0	REV SABTP (Process mode)	KU 001	MCW bit 0, reverse SAB tag, parity (SAB P1–5).
5	2	1	LCMPR (Process mode)	KU 001	MCW bit 1, start count on storage address compare (used with MCW bits 21–31).
5	2	2	REV SAFSP (Process mode)	KU 001	MCW bit 2, reverse serial adder full sum parity.
5	2	3	REV MRKP (Process mode)	KU 011	MCW bit 3, reverse mark parity.
5	2	0–3	CE TEST ADDR (Scan mode)	KU 011	MCW bits 0–3, address of ROS bit plane being tested (used for display only).
5	2	4	REV SARPA (Process mode)	KU 011	MCW bit 4, reverse storage address parity for byte 1 (SAC P 8–15).
5	2	4	LFTHF (Scan mode)	KU 011	Left half of word being scanned out contains the expected status of the trigger being tested.
5	2	5	REV SARPB (Process mode)	KU 011	MCW bit 5, reverse storage address parity for byte 2 (SAB P16–20).
5	2	5	UNCT (Scan mode)	KU 011	Unconditional terminate at end of current test.
5	2	6	LOG CNT (Process mode)	KU 021	MCW bit 6, start logout when FLT counter steps to zero.
5	2	6	CONDT (Scan mode)	KU 021	Conditional terminate, stop at end of current test if an error is encountered.
5	2	7	ERSLT (Scan mode)	KU 021	Expected result of the trigger being tested.
5	2	8	DSBL TMR	KU 021	MCW bit 20, disable internal timer (used for display only in scan mode and indicates a successful hardcore stop).
5	2	9–13	ADDR SEQUENCE	KU 101	Contents of address sequence register.
5	2	14–17	FLT COUNTER	KU 111	Contents of FLT counter.
5	2	18,19	FLT CHK	KU 271	FLT clock.
5	2	21–23	ROS TEST SEQ	KU 121	ROS test sequence, controls scan logic during a ROS test.
5	2	29	PASS	KU 391	An FLT or a ROS test has been completed and the expected result was obtained.
5	2	30	FAIL	KU 391	An FLT or a ROS test has been completed and the expected result was not obtained.
5	2	32	FLT STG ERR	KU 471	Any storage error detected while performing an FLT or a ROS test.
5	2	34	MMSC	KU 251	Maintenance mode stop clock.
5	2	35	BFR 1	KU 531	Buffer 1 (main storage 100–187) contains control information for FLT or ROS test being performed.
5	3	0–17	R REGISTER	RR 001	Contents of R register.
5	3	18–35	E REGISTER	RE 001	Contents of E register.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
5	4	0	S 0–31 32–63	RT 815	Gate S (0–31) to parallel adder A (32–63).
5	4	1	T 32–63 32–63 T	RT 807	Gate T (32–63) to parallel adder A(32–63) true.
5	4	2	T 32–63 32–63 C	AP 731	Gate T (32–63) to parallel adder A (32–63) complement.
5	4	3	T32–63 31–62 TL 1	RT 811	Gate T (32–63) to parallel adder A (31–62) true.
5	4	4	T32–63 31–62 CL 1	RT 811	Gate T (32–63) to parallel adder A (31–62) complement.
5	4	5	T32–47 48–63	RT 813	Gate T (32–47) to parallel adder A (48–63).
5	4	6	T48–63 48–63	RT 815	Gate T (48–63) to parallel adder A (48–63).
5	4	7	K00–31 32–63	RT 817	Gate K (00–31) to parallel adder A (32–63).
5	4	8	D 8–31 8–31 T	RT 803	Gate D (8–31) to parallel adder A (8–31) true.
5	4	9	D8–31 8–31 C	RT 803	Gate D (8–31) to parallel adder A (8–31) complement.
5	4	10	D8–31 7–30 T	RT 805	Gate D (8–31) to parallel adder A (7–30) true.
5	4	11	D8–31 7–30 C	RT 805	Gate D (8–31) to parallel adder A (7–30) complement.
5	4	12	D8–31 40–63 T	RT 801	Gate D (8–31) to parallel adder A (40–63) true.
5	4	13	D8–31 40–63 C	AP 811	Gate D (8–31) to parallel adder A (40–63) complement.
5	4	14	FMTO	RT 843	Gate LM to XY per E 13–15 – used when executing repack symbols instruction to move history or current data from old refresh memory to new refresh memory.
5	4	15	FMTN	RT 843	Gate LM to XY per E13–15 – used when executing repack symbol instruction to move new data from a sort bin to new refresh memory.
5	4	16	FMTW	RT 843	Gate LM to XY per E14, 15 – used when executing convert weather lines instruction to assemble the correct doubleword format in XY.
5	4	17	IC 40–63	RB 811	Gate IC (8–31) to parallel adder B (40–63).
5	4	18	A 0–31 32–63	RB 805	Gate A(0–31) to parallel adder B (32–63).
5	4	19	A4–7 4–7	RB 805	Gate A(4–7) to parallel adder B(4–7).
5	4	20	A8–31 8–31	RB 757	Gate A(8–31) to parallel adder B (8–31).
5	4	21	B32–63 32–63	RB 813	Gate B (32–63) to parallel adder B(32–63).
5	4	22	B 64–67 64–67	RB 761	Gate B (64–67) to parallel adder B (64–67).
5	4	23	A6–31 4–29	RB 811	Gate A (6–31) to parallel adder B (4–29).
5	4	24	B32–67 30–65	AP 745	Gate B (32–67) to parallel adder B (30–65).
5	4	25	B64–67 28–31	RB 757	Gate B (64–67) to parallel adder B (28–31).
5	4	26	EXCS 6 28–63	AP 737	Generate excess 6 decimal correction factor to parallel adder B (28–63), used while executing convert to decimal instruction.
5	4	27	F 4–7 60–63	RB 807	Gate F (4–7) to parallel adder B (60–63).
5	4	28	HOT 1 60	RB 807	Generate a 1 bit to parallel adder B (60) which effectively adds +8.
5	4	29	E8–11 56–59	RQ 801	Gate E(8–11) to parallel adder B (56–59).
5	4	30	E 12–15 60–63	RQ 801	Gate E (12–15) to parallel adder B (60–63).
5	4	31	E 8–11 60–63	RQ 801	Gate E(8–11) to parallel adder B (60–63).
5	4	32	Q 4–15 52–63	RQ 815	Gate Q (4–15) to parallel adder B (52–63).
5	4	33	Q 20–31 52–63	RQ 815	Gate Q (20–31) to parallel adder B (52–63).
5	4	34	Q 36–47 52–63	RQ 815	Gate Q (36–47) to parallel adder B (52–63).
5	4	35	Q 52–63 52–63	RQ 815	Gate Q (52–63) to parallel adder B (52–63).
5	5	1,2	STATE	FG 001	Operational state of CE.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
5	5	3–6	SCON	FC 001	Reconfiguration accepted from indicated CE.
5	5	7	ILOS	FC 061	CE will not issue logout stop signal to SE or DE.
5	5	10–20	SE SE/DE	FC 071	CE is able to communicate with indicated element.
5	5	23–26	CE	FC 191	CE is able to communicate with indicated element.
5	5	33–35	IOCE	FC 271	CE is able to communicate with indicated element.
5	6	0–35	DIAGNOSE ACCESSIBLE REGISTER MASK	FD 501	Indicated element is allowed to cause an external interruption in the CE.
6	1	0–35	PARALLEL ADDER LATCHES	AP 321	Contents of parallel adder latches (32–63).
6	2	0–8	MASKS	CT 011	Individual bytes of doubleword to be entered into main storage on a store operation.
6	2	10–14	LS ADDRESS REGISTER	LS 851	Contents of local storage address register.
6	2	15	LS WRITE	LS 812	CE is executing a micro-instruction to write into local storage.
6	2	16	INHIB STORE WRITE	RX 003	Inhibit storing into local storage.
6	2	17	TX TGR	DP 071	Multiply control trigger.
6	2	19–22	B REG	RB 641	Contents of B register 64–67.
6	2	24–26	ABC	CW 011	Contents of AB register byte counter.
6	2	28–31	PADDL	AP 671	Contents of parallel adder latches 64–67.
6	2	32	INSERT LS SIGN	RT 627	Gate result sign to local storage bus.
6	2	33–35	STC	CS 011	Contents of ST register byte counter.
6	3	1–8	SERIAL ADDER LATCHES	AS 001	Contents of serial adder latches.
6	3	10–35	INSTRUCTION COUNTER	CA 001	Contents of instruction counter 8–31.
6	4	1–35	DIAGNOSE ACCESSIBLE REGISTER	FD 001	An external interrupt request caused by an element check in the indicated device.
6	5	1–4	STOR UNIT CHECK ID	MC 961	Binary identification of SE or DE gating data to storage data bus out or causing time out pulse to be activated in the CE.
6	5	5	360 MODE	KM 201	CE is in 360 mode of operation.
6	5	6	TEST MODE	PX 331	CE is in state 0 and TEST switch is in TEST.
6	5	7	SE STOP 360	KM 201	Select pulse has been sent to a SE that is stopped while the CE is operating in 360 mode.
6	5	10	SAB PTY CHK	MA 951	Parity error is detected in SAB.
6	5	11	SDBI PTY CHK	MB 273	Parity error detected on SDBI.
6	5	12	STG TO	MC 753	SE or DE did not respond to a select signal within prescribed time.
6	5	13	STG ADDR CHK	MC 756	Storage address check signal received from an SE or a DE.
6	5	14	STG DATA CHK	MC 756	Storage data check signal received from an SE or a DE.
6	5	15	SDBO FETCH CHK	MC 941	Parity error detected on SDBO during a fetch cycle.
6	5	16	LOS SENT	MC 923	Logout stop signal sent to an SE or a DE.
6	5	19	IOCE CHK RESP	KX 311	Check response signal received from IOCE (error condition).
6	5	20	LS BUS CHK	BF 441	Parity error detected in local storage out bus.
6	5	21	CCR PTY CHK	FC 361	Parity error detected in CCR.
6	5	22	ATR PTY CHK	FA 141	Parity error detected in ATR.
6	5	23	PSBAR PTY CHK	MP 441	Parity error detected in PSBAR.
6	5	24	PSBAR NOT CONF	MP 531	CE does not have an SE available for its PSA.
6	5	25	PSA ALT	MP 531	'Go to Alt PSBAR' signal and 'Rem Alt' latch set.
6	5	26	SPLIT LOGOUT	MC 791	Invalid address or storage timeout detected during logout causes CE to step PSBAR to alternate and start new logout.
6	5	28	LOG ROS CHK	KU 231	ROS address outside logout microprogram range (A00–A1F) detected during logout.

Table 2-2. Roller Indicators (continued)

Roller Number	Roller Position	Bit Position	Indicator Name	ALD Reference	Condition Indicated
6	5	29	LOG ADDR CHK	MA 901	Address outside PSA detected on SAB during logout.
6	5	30	CE LOG REQ	KW 071	Logout request signal received from a CE.
6	5	31	RDD TO	KN 281	Data not available on direct control bus within prescribed time during read direct operation.
6	6	1–4	LOGOUT OR WRAP SELECTED STG ID	KU 041	Identify (binary) SE or DE selected during logout, wrap DE, or force DG request operation.
6	6	5–8	DG SELECTED	KU 061	Identify (binary) DG specified during wrap DE or force DG request operations.
6	6	10–15	CVG SELECTED	KU 071	Identify (numeric) CVG specified during wrap DE or force DG request operation.
6	6	16	REV NORM OP	KU 081	Reverse 'normal op'.
6	6	17	FORCE DG REQ	KU 081	Force DG request.
6	6	19	DIAG SE 1	KU 091	Blocks 'invalid address decoded' which is activated when SAB bit 8 = 1.
6	6	20	INV EXT PTY	KU 091	Invert P0–7 of external register.
6	6	21	RST CHKS	KU 091	Reset check register bits.
6	6	22	WRAP DE	KU 091	Wrap DE operation in progress.

2.1.6 Panel F

1. REPEAT switch. This switch causes the FLT or ROS test in storage to be repeated or allows searching for a particular test and repeating that test. The operation is as follows:
   a. REPEAT switch in REPEAT position and depression of START pushbutton will cause the FLT or ROS test in storage to be executed repeatedly.
   b. REPEAT switch in REPEAT position, test number in DATA switches (48–63), FLT tape rewound, and depression of STORE, then LOAD pushbuttons causes test number to be stored in T, FLT tape to be searched, and test to be loaded and executed repeatedly.
2. ROS/PROC/FLT switch. This switch provides two modes of testing. DISABLE INTERVAL TIMER switch must be in DISABLE position when running either test.
   a. FLT position: CE is conditioned for running FLTs.
   b. PROC (process) position: normal position for CE processing.
   c. ROS position: CE is conditioned for running ROS tests.
3. DEFEAT INTERLEAVING switch. This three-position lever switch performs the following functions:
   a. PROC position: Locations of consecutive doublewords are alternated between two basic storage modules (BSM) within an SE or a DE (interleave mode).
   b. No REV position: Locations of consecutive doublewords are within one BSM of an SE or a DE (defeat interleave mode).
   c. REV position: Locations of consecutive doublewords are within one BSM of an SE or a DE, and odd and even BSMs are interchanged.
4. INHIBIT CE HARD STOP switch. When this switch is set to INHIBIT CE HARD STOP position, conditions that cause the CE to enter hard-stop state are prevented from doing so.
5. DISABLE INTERVAL TIMER switch. When this switch is set to DISABLE INTERVAL TIMER position, the interval timer is not decremented.
6. STORAGE SELECT switch. This switch has three positions:
   a. MAIN: Main storage is selected for manually storing or displaying data.
   b. LOCAL: Local storage (LS) is selected for manually storing or displaying data.
   c. MAIN BYTE: Main storage is selected for manually storing or displaying data. The byte selected by ADDRESS switches 21–23 is the only byte affected by a manual store operation.
7. ADDRESS COMPARE switch. This switch has three positions:
   a. PROC: A sync pulse is available on a coaxial connector at the front of gate C whenever there is an equal compare between storage address bus and ADDRESS switches 9–28.
   b. STOP: The CE stops at the end of the instruction