This manual contains the maintenance-oriented and recall diagrams referenced in the companion 7201-02 Computing Element PETOM (Form SFN-0201) and in the 7201-02 Computing Element FEMM (Form SFN-0203).

The diagrams in this manual are arranged into six categories:

Category 1. Diagnostic Techniques
Category 2. Overall Data Flow
Category 3. Data Flow by Instruction Class
Category 4. Functional Units
Category 5. Operations
Category 6. Manual Controls and Maintenance Facilities

All diagrams are in numerical order. The first digit of the diagram number reflects the category; for example, Diagram 4-210 belongs to Category 4, Functional Units. A category may be further subdivided into functional groups; for example, in Category 4, the diagrams have been grouped as follows:

Group 2. ROS
Group 3. Data and Control Registers

Group 4. Local Storage
Group 5. Serial and Parallel Adders
Group 6. Status and Control Triggers
Group 7. SCI

Prerequisite and companion manuals are:

Prerequisite Manuals
- 9020E System Introduction, Theory of Operation Manual, Form SFN-0103
- 9020D System Introduction, Theory of Operation Manual, Form SFN-0104

Companion Manuals
- 7201-02 Computing Element, Theory of Operation Manual, Form SFN-0201
- 7201-02 Computing Element, Maintenance Manual, Form SFN-0203
- 7201-02 Computing Element, Installation Manual, Form SFN-0204
- 7201-02 Parts Catalog, Form SFN-0205

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*Note: 1052 Adapter is used only with the 9020E configuration.

ABBREVIATIONS

ABC All register byte counter ac alternating current ACR Automatic Carrier Return ad address, addressed, addressing ALD automated logic diagram ALTN Alternate amp amperes APSA alternate preferential storage area ASC address store computer ATC air traffic control ATN alternate test number ATR address translation register Atmn attention Aux Auxiliary Magnet BCD binary-coded decimal BCU bus control unit (alternate terminology for SCI) block BR brightness BSM basic storage module C capacitor CAS control automation system CAW named address word CB circuit breaker CC configuration code, also Configuration Console CCC Central Computer Complex CCR configuration control register CCCW channel command word CE Controlling Element Chaarct Choaarct claarct command system logic diagram Cmd command CPU Central Processing Unit (alternate terminology for CE) CR divide or Carrier Return CROS negative read-only storage CT channel status word CTC conditional terminate CU Control Unit CVG Character Vector Generator DA dark DAB darkable register address register DAC digital-to-analog converter DAE darkenable register address enable DAF darkenable register address mask DAU Data Adapter Unit dc direct current DCP Display Channel Processor DFE Digital End ece decimal decimal divide dec ef decimal overflow DG Display Generator Disc disconnect delay D10 display dark disable DX first byte in a series of destination bytes DX+ second byte in a series of destination bytes DX- third byte in a series of destination bytes ELC element check end op end operation EO end of block EOL End-of-Line EPO emergency power off ERLST expected result EXC Executive Control Program exp on/off exp on/off exp on/off exp on/off F fume FEDOM Field Engineering Maintenance Directions Manual FEDOM Field Engineering Manual of Instruction FEMM Field Engineering Maintenance Manual FETOM Field Engineering Theory of Operation Manual FETOM Field Engineering Operation Manual fault-point overflow FLT fault locating test flash dir floating-point divide PMFTON Format New PMFTOF Format Old PMFW Format Weather FPR floating-point register frac fraction
GIS  general initialization sequence
GPR  general-purpose register
hex  hexadecimal
Hz  Hertz
IC  instruction counter
ICR  inhibit carrier return
IDES  inhibit display element stop
I-Fetch  instruction fetching
ILC  instruction length code
ILOG  inhibit login stop
Init  initial
I/O  input/output
IOCE  Input/Output Control Element
IPL  initial program load
K  kilo; also relay
kHz  kilohertz
LAB  logical address bus
LADS  Logic Automation Documentation System
LAL  local storage address latch
LAR  local storage address register
LC  lower case
LF  line feed
LOG  login stop
LS  local store
LSWR  local storage working register
MACH  maintenance and channel (storage)
max  maximum
MC  machine check
MCW  maintenance control word
MHz  megahertz
MMSC  maintenance mode stop clock
Mpla  Multiple
MPR  multiplier
MPX  multiplex
ms  millisecond
NDT  new descriptor tables
no op  no operation
NRM  new refresh memory
NRMA  new refresh memory address
ns  nanosecond
Obs  on battery signal
QDT  old descriptor tables
op code  operation code
op  operation
opend  opened
ORM  old refresh memory
ORMA  old refresh memory address
OTC  out of tolerance check
P  parity
PAA  parallel adder A-side
PAB  parallel adder B-side
PAL  parallel adder latch
PB  pushbutton
pf  picofarad
PK  power contactor
PP  partial product
PQ  partial quotient
prw op  privileged operation
proc  program
prog  program
PROSAR A  previous read-only storage address register A
PROSAR B  previous read-only storage address register B
PS  power supply
PSA  preferential storage address
PSBAR  preferential storage base address
PSW  program status word
PVD  Plan View Display
R  register
RCU  Reconfiguration Control Unit
reg  register
RKM  Radar Keyboard Multiplexor
ROS  read-only storage
ROSAR  read-only storage address register
ROSBR  read-only storage backup register
ROSISR  read-only storage data register
RST  Reset
SAA  serial adder A-side
SAB  storage address bus, also serial adder B-side
SAL  serial adder latch
SATR  set Address Translation Register
SB  serial adder bus
SBB  serial adder bus B
SC  System Console
SCI  storage control interface
SCON  set Configuration Control Register
SCOPEX  scope index
SCR  silicon-controlled rectifier
SDR  storage data bus in
SDBO  storage data bus out
SE  Storage Element
Sel  select
Serv  service
Sign  significance
SLT  solid logic technology
SMAC  system maintenance monitor console
SMS  standard modular system
SRS  scan out read-only storage
spec  specification
SRL  Systems Reference Library
SSU  storage switching unit
STAT  status trigger
STC  ST register byte counter
str  storage
sync  synchronizing
T  transformer
TC  time clock (interval timer)
TCU  tape control unit
TDX  table byte specified by DX
TDX+1  table byte specified by DX+1
TIC  transfer in channel
TN  test number
TR  tilt/rotate
TU  tape unit
uc  upper case
uf  microfarad
usec  microsecond
UT  unconditional terminate
V  volt
VFL  variable-field length
VFR  visual flight rules
Xlat  translate
Y  greater than or equal to
Y  greater than or equal to
Z  less than or equal to
Z  less than or equal to
a  equal to
a  not equal to
and
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Diagram 1-3: FLT Flowchart
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Diagram 3-2. Floating-Point Instruction Data Flow
Diagram 3-3. Decimal and Logical Instruction Data Flow
Diagram 3-5. Status Switching Instruction Data Flow
Diagram 3-6. Input/Output Instruction Data Flow
Diagram 4-2. Reference Oscillator

Notes:
1. Heavy portion of timing signals indicates the active portion for the signal function.
2. The two letter notation within the AND's is the block which number an AID KO207.
   *Inverter block is part of logic block.*
Diagram 4-3. CE Clock Signal Generator

- If line is positive, oscillator output is positive and not running. When line goes negative, oscillator output goes negative and starts stable oscillation.

- Not inhibit OSC, On Wrap, Or Logout

- Not Wrap Mode
  - Inhibit Osc Set Outstanding

- Hardstop Inhibit OSC

- Frequency Alteration Switch

- Frequency Alteration Circuit

- Machine reset

- To Diagram 4-2

- 5.0-mHz OSCILLATOR
  - Adjust for symmetrical 100-ns/100-ns clock signal.
  - Adjust for 200-ns period clock signal (Null-Comparator)

- Symmetry Observation Point

- Gated Oscillator
  - (Basic Clock Pulse)

- 5.0-mHz REFERENCE
  - (From crystal-controlled; same as shown in Diagram 4-2.)
  - Null Observation Point

- 5.0-mHz Comparator Circuit

- 500-kHz Low-Pass Filter

- Filter converts square wave input to a sine wave.
Diagram 4-101. ROSAR (0-5) Logic
Diagram 4-104. ROSAR (13) Logic
Diagram 4-105. ROS Addressing and Data Flow (Sheet 1 of 2)
Diagram 4-106. Array Drivers

Select 0

Select 1

Select 2

Array Drivers
3 through 10
Not Shown

Select 19

Select 20

Select 21

Drive 0 PS-QPA

Drive 1 PS-QPF

Drive 43 PS-QPA

Drive 43 PS-QPF

Drive 43 PS-QPF

Drive 43 PS-QPF

Drive 43 PS-QPF
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Diagram 4-201. Q-Register B-Field Transfer Controls

Diagram 4-202. R-Register Transfer to LAL
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Diagram 4-212. XY Register Parity Prediction Logic
Diagram 4-213. Select Register - Select Signal Generation and Response Route.
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Diagram 4-302. 9020 Out Bus to LS Data Bus Getting Logic.
Diagram 4-303, LS Bus Parity Generation or Check
Diagram 4-402. Carry Lookahead Logic, SAL(0-3)

Diagram 4-403. Decimal Add 6 Logic
Diagram 4-404. Decimal Correction Logic For SAL (0-3)

Diagram 4-405. Invalid Digit Logic
Diagram 4-406. Logical Functions, SAL (0)

Diagram 4-407. Serial Adder Parity Predict Logic
Diagram 4-408. Serial Adder Product-Quotient Bit Logic

A. T-Field Gate Control Trigger;
   A' Micro-order (1111);
   Decoder T11;
   Gate K102-63 to Parallel Adder B-Side (32-63).

B. U-Field Gate Control Trigger;
   A' Micro-order (1110);
   Decoder U13;
   Gate T128-63 to Parallel Adder A-Side (32-63).

Diagram 4-409. Gate Control Triggers for 'B + T' Micro-order
Diagram 4-10. Parallel Adder Bit-Position Logic (Bit 47)

Note: A "not group 4 carry" signal indicates that an extored carry from group 4 progresses 4 positions. All, 48, 56, and 63 has not occurred, thus allowing a propagated carry (carry-latch-group 15) to enter bit position 47. The diagram indicates: 1. Propagation (carry group 4) 2. Progression (carry group 4) 3. Propagation (carry group 3) 4. Progression (carry group 3) 5. Propagation (carry group 2) 6. Progression (carry group 2) 7. Propagation (carry group 1) 8. Progression (carry group 1) 9. Propagation (carry group 0) 10. Progression (carry group 0)
Diagram 4-411. Parallel Adder Carry Lookahead Logic
Diagram 4-412. Parity Generation, PAL (48-55)

**Parity Prediction, PAL(48-55)**

- **Input Channels:**
  - 48 Hal-Sum
  - Not 48 Hal-Sum
  - Not 48 Bit Transf
  - Not 5 Bit Transf
  - Not 5 Bit Transf

- **Logic Blocks:**
  - A: OR
  - B: AND

- **Parity Detection Logic:**
  - **A.** Parity Prediction, PAL(48-55)
    - Parity Predicted
    - PAL(48-55)

- **Shift Logic:**
  - **B.** Parity Latch-Shift Logic, PAL(48-55)
    - Right 4-Shift
    - Left 4-Shift

- **Output:**
  - Parity
  - FI Clock Extended
  - Zero Shift
  - Not 48-55 Parity

---

**Notes:**
- Duplicate logic is used for generating parity-predicted signals of opposite polarity simultaneously (without use of additional inverter function).
Diagram 4-13. Parallel Adder Half-Sum Checking Logic, PA (48-55)
Diagram 4-414, Parallel Adder Full-Sum Checking Logic, PA(48-55)
Diagram 4-415. Parallel Adder Excess 6 Logic

Diagram 4-416. Parallel Adder Set-Condition-Code Logic

Note: This diagram illustrates how the condition codes are set; it is not intended to be a detailed diagram.
Diagram 4-501. STAT B Logic
Diagram 4-602. Address Decode and Gating Logic
Diagram 4-603. SCI Control Logic for CE Clock
Diagram 4-605. Storage Timeout Logic

Notes:
1. "Storage Timeout" is activated if "Select outstanding" remains active through two 80-cycle pulses.
2. "Select outstanding" may come at any time for the example shown; it is for the best output of time necessary to see "Storage Timeout".
3. "Select outstanding" is deasserted by "select" from storage.
Diagram 4-609. Page Control Logic and Timing
Diagram 4-610. SAB Parity Conversion Logic
Diagram 4-611. Servicing of Storage Requests in Single-Cycle Mode (Sheet 2 of 2)
Diagram 4.612. Servicing of Storage Requests in Single-Cycle Mode