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## I-FETCH

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# LECTURE NOTES FROM THE FAA ACADEMY 9020 COURSE
"IBM 9020D/E SYSTEMS 7201-02 COMPUTING ELEMENT"
(ENHANCED IBM S/360 MODEL 65)

Coloured-in by Chris Bigos in Oklahoma USA 1979
Scanned in by Chris Bigos in London UK 2012
Basic Computer

1-1
ROSAR
GATE DRIVER STROBE
GATE WORD SELECT STROBE
SENSE LATCH STROBE
SENSE LATCHES
ROSDR 2-42 INGATE REG.
ROSDR LATCHES
ROSDR 69-84 (OUTGATES)

ROSA LATCHES

ROS TIMING See FETOM 1-27
1-4
MACHINE CYCLE

P15
P15-PO
P11-P10
P2-P1
P16-P12

CLOCK
Not CLOCK

ROS SENSE LATCHES
OUTGATE MICRO-ORDERS
INGATE MICRO-ORDERS

FIELDS

A. P2-P1 (A7 ONLY)
B. P11-P10
C. P2-P1 (C3 ONLY)
D. P2-P1 (D1, D2, D3)
E. P2-P1
F. P2-P1

G. P2-P1
H. P2-P1
I. P2-P1
J. P2-P1
K. P2-P1
L. P16-P12
M. P2-P1
N. P2-P1

P11-P10 (ALL OTHERS)
P11-P10
P11-P10 (ALL OTHERS)
P11-P10

P. P2-P1
Q. P2-P1
R. P2-P1
S. P2-P1
T. P2-P1
U. P2-P1
V. P2-P1
W. P2-P1

43463/AAC-942E (12/76)

ROS FIELD TIMING

SEE FETOM P.1-20
Any ROS address \( \text{X'O8' to X'FF'} \) is invalid. Any ROS address above \( \text{X'D7'} \) is invalid.

READ ONLY STORAGE ADDRESS REGISTER

MSB

0 1 2 3 4 5 6 7 8 9 0 1

LSB

\[ \text{X'943'} \]

SELECTS UPPER OR LOWER WORD

Bit 11 = 1, LOWER (ODD) WORD
Bit 11 = 0, UPPER (EVEN) WORD.

Eg.: ADDR. "FA0"

GATE - 1 = "D"

PLANE - F = "15"

DRIVER - 3F = "63"

SEL. LINE = "A" < 10

1 PLANE = "3"

WORD = 0 = "UPPER"

* QUARTER PLANES ARE NUMBERED LEFT TO RIGHT FROM PRESSURE PLATE SIDE.
DATA MOVEMENT SCHEME

Trimming on Handout 4-15.
ROS WORD

ASSUME ROS SENSE LTH BIT 9

0 - 1 - 0 - 0

TIME

W X Y Z

FIG 1 - 9 LOCATIONS
<table>
<thead>
<tr>
<th>IPSW LOC</th>
<th>IPSW</th>
<th>INST. ADR.</th>
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<tbody>
<tr>
<td>000000</td>
<td>XXXX X X X X X X</td>
<td>X X 0 0 1 0 0 0</td>
</tr>
<tr>
<td>001000</td>
<td>(BALR) R1 R2 (IM) R1 R3</td>
<td>B D I S (ST) R1 X</td>
</tr>
<tr>
<td>001008</td>
<td>B D I S (AP) L1 L2</td>
<td>B1 D I S B2 D I S</td>
</tr>
<tr>
<td>001010</td>
<td>(SCON) R1 R2 (SATR) R1 R2</td>
<td>Reg 0 (ATR 1 Ms)</td>
</tr>
<tr>
<td>001018</td>
<td>Reg 1 (ATR 2, Select)</td>
<td>Reg 2 (Config. Ms)</td>
</tr>
<tr>
<td>001020</td>
<td>Reg 3 (Config. Ms)</td>
<td>Reg 4 (Rl for ST)</td>
</tr>
<tr>
<td>001028</td>
<td>Reg 5 (X for ST)</td>
<td>AP Op 1</td>
</tr>
<tr>
<td>001030</td>
<td>AP Op 2</td>
<td>Stor Wd for Reg 4 (ST)</td>
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Machine Language Program
1-14
14
Instruction Request During NEOP and BEOP

Instruction Request During NEOP and BEOP

2-3

17
1. HARDWARE DETECTS Q REFILL PRIORITY.
2. ISSUE 3-CYCLE REQUEST PER IC.
3. START I-FETCH SEQUENCERS.
4. SET UP EXCEPTIONAL CONDITION TO I-FETCH.

1. BLOCK μ-ORDER E(02-07) → ROA.
2. EXCEP μ-ORDER FORCES ROSAR TO 034.

1. WHEN IF-1 LTH SETS, GATE IC TO PAB, AND SET PAA 60.
2. WHEN IF-2 LTH SETS, GATE PAL (40-53) TO IC.
3. RASCR μ-ORDER "ANDED" WITH IF-2 LTH SETS IF-1 TCR AND IF-1 LTH.
4. ISSUE MS REQxD-3 FOR OPERAND.
5. E(02-07) → ROA.

1. MS 1 T GATES SDB0 (32-63) TO T.
2. ALSO GATES SDB0 (00-15) TO R.

IF IC(21-22) = 00.

IF-3 LTH "ANDED" WITH IF-1 LTH GATES SDB0 TO Q. INSTR. WORD COMES FROM S.E.
Exception μ-Order For "Q" Refill Priority (ROS 034) (RS-S1 Format)
SPEC μ-Order (K31) Force ROS to Ø1Ø

2-12